Kindly **add** the following claims:

--151. A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation of the memory device comprises:

receiving an external clock signal;

receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a read request;

receiving a first read request synchronously with respect to a rising edge transition of the external clock signal; and

outputting the amount of data, in response to the first read request, the amount of data corresponding to the block size information.

152. The method of claim 151 wherein the block size information defines an amount of data to be input by the memory device in response to a write request, the method further including:

receiving a first write request synchronously with respect to a transition of the external clock signal; and

inputting the amount of data, in response to the first write request, the amount of data corresponding to the block size information.

153. The method of claim 152 wherein a first portion of data is sampled, in response to the first write request, after a delay time transpires.

154. The method of claim 151 wherein the amount of data is output synchronously with respect to the external clock signal.

155. The method of claim 154 wherein a first portion of data is output synchronously with respect to a rising edge transition of the external clock signal and a second portion of data is output synchronously with respect to a falling edge transition of the external clock signal.

156. The method of claim 151 wherein the first read request is specified by an operation code.

157. The method of claim 156 wherein the operation code includes precharge information.

158. The method of claim 156 wherein the operation code is included in a request packet.

159. The method of claim 158 wherein the block size information and the operation code are both included in the same request packet.

160. The method of claim 158 wherein the request packet includes address information.

161. The method of claim 151 wherein the block size information is sampled synchronously with respect to the external clock signal.

162. The method of claim 151 further including:

receiving a code which is representative of a number of clock cycles of the external clock signal to transpire before the memory device responds to the first read request; and

storing the code in a register.

163. The method of claim 162 wherein the memory device outputs a first portion of data after the number of clock cycles of the external clock signal transpire.

164. The method of claim 151 wherein the block size information is a binary code.

165. A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells, the method of controlling the memory device comprises:

providing block size information to the memory device, synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request; and

issuing a first read request to the memory device, wherein the memory device receives the first read request synchronously with respect to a transition of the external clock signal.

166. The method of claim 165 further including receiving the amount of data from the memory device.

167. The method of claim 165 further including providing a code to the memory device, wherein the code is representative of a number of clock cycles of the external clock signal to transpire before the memory device responds to the first read request.

168. The method of claim 167 further including providing a set register request to the memory device, wherein the memory device stores the code in a register in response to the set register request.

169. The method of claim 165 wherein the first read request is specified by an operation code.

170. The method of claim 169 wherein the operation code includes precharge information.

171. The method of claim 169 wherein the operation code is included in a request packet.

172. The method of claim 171 wherein the block size information is included in a request packet.

173. The method of claim 171 wherein the block size information and the operation code are both included in the same request packet.

174. The method of claim 171 wherein the request packet further includes address information.

175. The method of claim 165 wherein the block size information is a binary code.

176. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to receive block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request; and

a plurality of output drivers to output the amount of data corresponding to the block size information, wherein the first amount of data is output in response to the read request.

177. The memory device of claim 176 wherein the amount of data is output synchronously with respect to the external clock signal.

178. The memory device of claim 177 wherein a first portion of data is output synchronously with respect to a rising edge transition of the external clock signal and a second portion of data is output synchronously with respect to a falling edge transition of the external clock signal.

179. The memory device of claim 176 wherein the first read request is specified by an operation code.

180. The memory device of claim 179 wherein the operation code is included in a request packet.

181. The memory device of claim 180 wherein the block size information is included in a request packet.

182. The memory device of claim 181 wherein the block size information and the operation code are included in the same request packet.

183. The memory device of claim 179 wherein the operation code includes precharge information.

184. The memory device of claim 176 further including a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before the memory device responds to a read request.

185. The memory device of claim 176 wherein the block size information defines an amount of data to be input in response to a write request.

186. The memory device of claim 185 wherein the input receiver circuitry samples a first portion of the amount of data in response to the write request.